

CAV93C66

4 Kb Microwire Serial CMOS EEPROM

Description

The CAV93C66 is a 4 Kb CMOS Serial EEPROM device which is organized as either 256 registers of 16 bits (ORG pin at V_{CC}) or 512 registers of 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The device features sequential read and self-timed internal write with auto-clear. On-chip Power-On Reset circuitry protects the internal logic against powering up in the wrong state.

Features

- Automotive Temperature Grade 1 (–40°C to +125°C)
- High Speed Operation: 2 MHz
- 2.5 V to 5.5 V Supply Voltage Range
- Selectable x8 or x16 Memory Organization
- Self-timed Write Cycle with Auto-clear
- Sequential Read
- Software Write Protection
- Power-up Inadvertent Write Protection
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-lead SOIC and TSSOP Packages
- These Devices are Pb-Free, Halogen Free/BFR Free, and RoHS Compliant

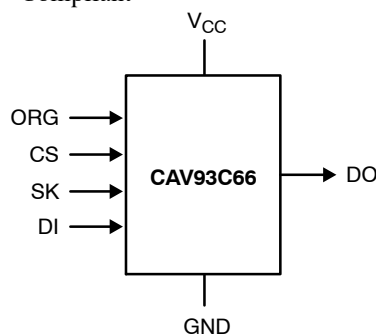


Figure 1. Functional Symbol

Note: When the ORG pin is connected to V_{CC}, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the x16 organization.



ON Semiconductor®

<http://onsemi.com>

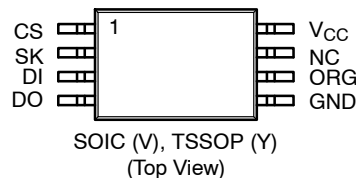


SOIC-8
V SUFFIX
CASE 751BD



TSSOP-8
Y SUFFIX
CASE 948AL

PIN CONFIGURATIONS



PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V _{CC}	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

CAV93C66

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- The DC input voltage on any pin should not be lower than -0.5 V or higher than $V_{CC} + 0.5$ V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than $V_{CC} + 1.5$ V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

- These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- Block Mode, $V_{CC} = 5$ V, 25°C.

Table 3. D.C. OPERATING CHARACTERISTICS ($V_{CC} = +2.5$ V to +5.5 V, $T_A = -40$ °C to +125°C unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Supply Current (Write)	$V_{CC} = 5.0$ V		1	mA
I_{CC2}	Supply Current (Read)	DO open, $f_{SK} = 2$ MHz, $V_{CC} = 5.0$ V		500	μA
I_{SB1}	Standby Current (x8 Mode)	$V_{IN} = GND$ or V_{CC} CS = GND, ORG = GND		5	μA
I_{SB2}	Standby Current (x16 Mode)	$V_{IN} = GND$ or V_{CC} CS = GND, ORG = Float or V_{CC}		3	μA
I_{LI}	Input Leakage Current	$V_{IN} = GND$ to V_{CC}		2	μA
I_{LO}	Output Leakage Current	$V_{OUT} = GND$ to V_{CC} CS = GND		2	μA
V_{IL1}	Input Low Voltage	4.5 V $\leq V_{CC} < 5.5$ V	-0.1	0.8	V
V_{IH1}	Input High Voltage	4.5 V $\leq V_{CC} < 5.5$ V	2	$V_{CC} + 1$	V
V_{IL2}	Input Low Voltage	2.5 V $\leq V_{CC} < 4.5$ V	0	$V_{CC} \times 0.2$	V
V_{IH2}	Input High Voltage	2.5 V $\leq V_{CC} < 4.5$ V	$V_{CC} \times 0.7$	$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	4.5 V $\leq V_{CC} < 5.5$ V, $I_{OL} = 3$ mA		0.4	V
V_{OH1}	Output High Voltage	4.5 V $\leq V_{CC} < 5.5$ V, $I_{OH} = -400$ μA	2.4		V
V_{OL2}	Output Low Voltage	2.5 V $\leq V_{CC} < 4.5$ V, $I_{OL} = 1$ mA		0.2	V
V_{OH2}	Output High Voltage	2.5 V $\leq V_{CC} < 4.5$ V, $I_{OH} = -100$ μA	$V_{CC} - 0.2$		V

Table 4. PIN CAPACITANCE ($T_A = 25$ °C, $f = 1.0$ MHz, $V_{CC} = +5.0$ V)

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT} (Note 4)	Output Capacitance (DO)	$V_{OUT} = 0$ V			5	pF
C_{IN} (Note 4)	Input Capacitance (CS, SK, DI, ORG)	$V_{IN} = 0$ V			5	pF

- These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

CAV93C66

Table 5. POWER-UP TIMING (Notes 5, 6)

Symbol	Parameter	Max	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
6. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 6. A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50 ns		
Input Pulse Voltages	0.4 V to 2.4 V	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	
Timing Reference Voltages	0.8 V, 2.0 V	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	
Input Pulse Voltages	$0.2 V_{CC}$ to $0.7 V_{CC}$	$2.5\text{ V} \leq V_{CC} \leq 4.5\text{ V}$	
Timing Reference Voltages	$0.5 V_{CC}$	$2.5\text{ V} \leq V_{CC} \leq 4.5\text{ V}$	
Output Load	Current Source I_{OLmax}/I_{OHmax} ; $CL = 100$ pF		

Table 7. A.C. CHARACTERISTICS ($V_{CC} = +2.5\text{ V}$ to $+5.5\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
t_{CSS}	CS Setup Time	50		ns
t_{CSH}	CS Hold Time	0		ns
t_{DIS}	DI Setup Time	100		ns
t_{DIH}	DI Hold Time	100		ns
t_{PD1}	Output Delay to 1		0.25	μs
t_{PD0}	Output Delay to 0		0.25	μs
t_{HZ} (Note 7)	Output Delay to High-Z		100	ns
t_{EW}	Program/Erase Pulse Width		5	ms
t_{CSMIN}	Minimum CS Low Time	0.25		μs
t_{SKHI}	Minimum SK High Time	0.25		μs
t_{SKLOW}	Minimum SK Low Time	0.25		μs
t_{SV}	Output Delay to Status Valid		0.25	μs
SK_{MAX}	Maximum Clock Frequency	DC	2000	kHz

7. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

Device Operation

The CAV93C66 is a 4096-bit nonvolatile memory intended for use with industry standard microprocessors. The CAV93C66 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The device operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation. The serial communication protocol follows the timing shown in Figure 2.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical “1” start bit, a 2-bit (or 4-bit) opcode, 8-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations). The instruction format is shown in Instruction Set table.

Table 8. INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A8-A0	A7-A0			Read Address AN – A0
ERASE	1	11	A8-A0	A7-A0			Clear Address AN – A0
WRITE	1	01	A8-A0	A7-A0	D7-D0	D15-D0	Write Address AN – A0
EWEN	1	00	11XXXXXXXX	11XXXXXXXX			Write Enable
EWDS	1	00	00XXXXXXXX	00XXXXXXXX			Write Disable
ERAL	1	00	10XXXXXXXX	10XXXXXXXX			Clear All Addresses
WRAL	1	00	01XXXXXXXX	01XXXXXXXX	D7-D0	D15-D0	Write All Addresses

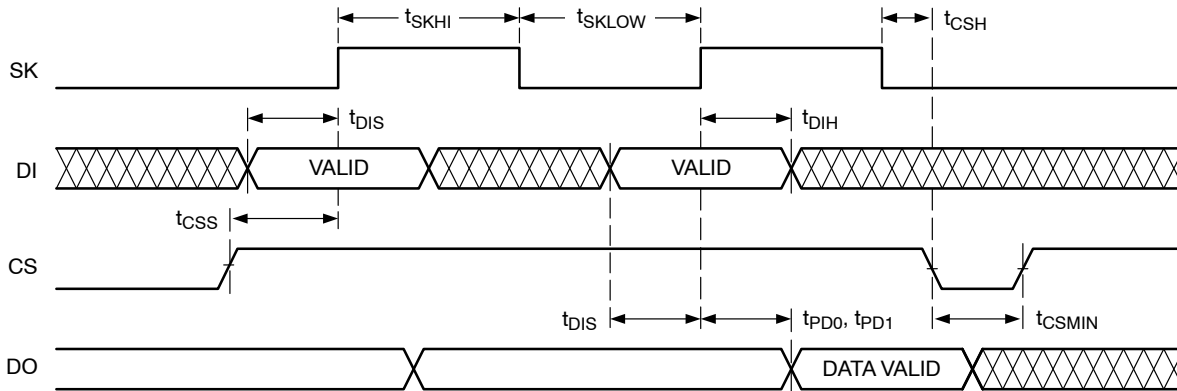


Figure 2. Synchronous Data Timing

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAV93C66 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

For the CAV93C66 after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data

word is preceded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit. The READ instruction timing is illustrated in Figure 3.

Erase/Write Enable and Disable

The device powers up in the write disable state. Any writing after power-up or after an EWDS (erase/write disable) instruction must first be preceded by the EWEN (erase/write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAV93C66 write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 4.

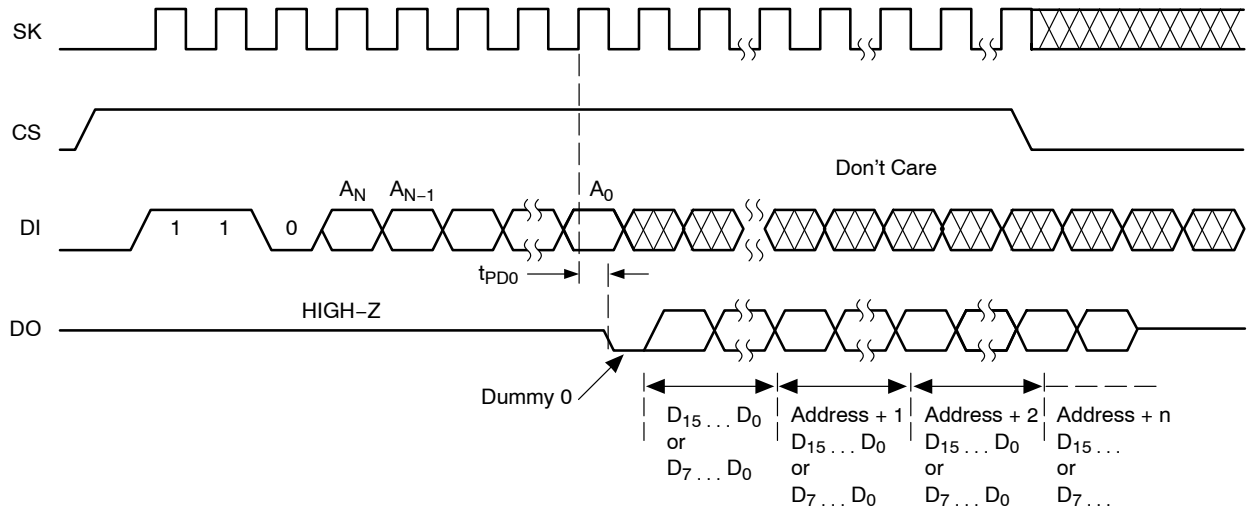


Figure 3. READ Instruction Timing

CAV93C66

Write

After receiving a WRITE command (Figure 5), address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C66 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN} (Figure 6). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C66 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

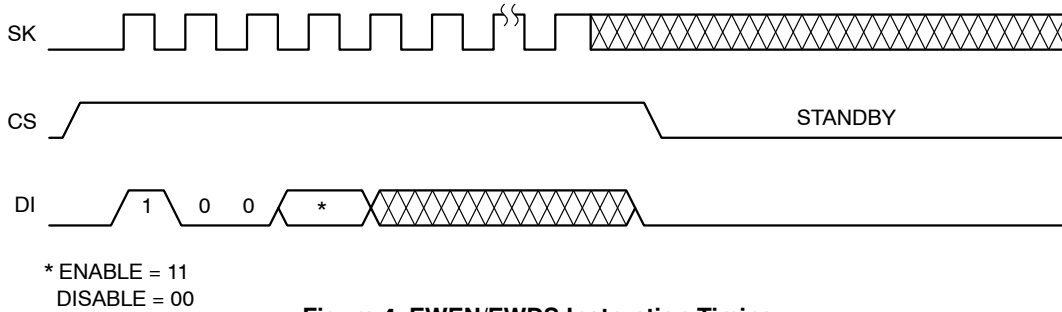


Figure 4. EWEN/EWDS Instruction Timing

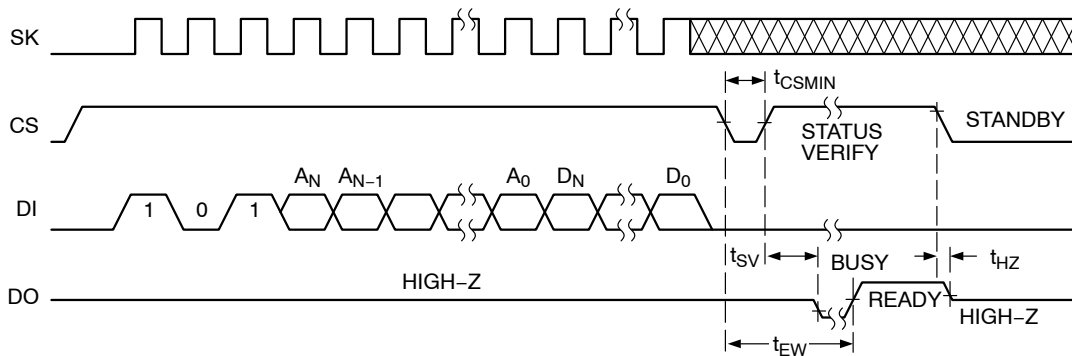


Figure 5. Write Instruction Timing

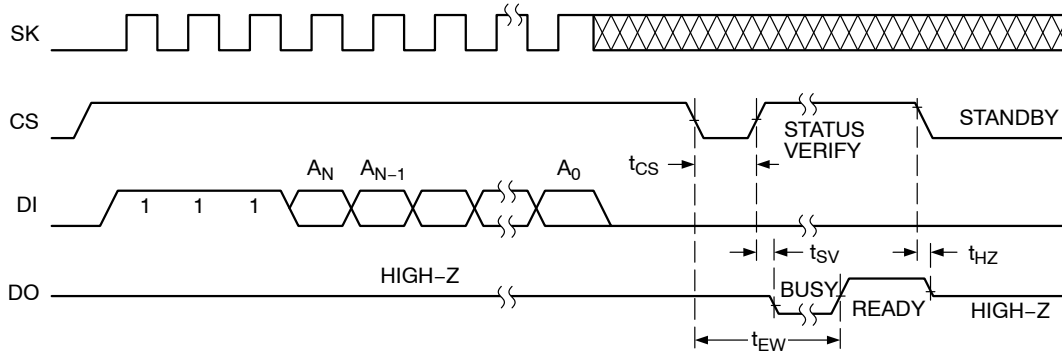


Figure 6. Erase Instruction Timing

CAV93C66

Erase All

Upon receiving an ERAL command (Figure 7), the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the device can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} (Figure 8). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the device can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

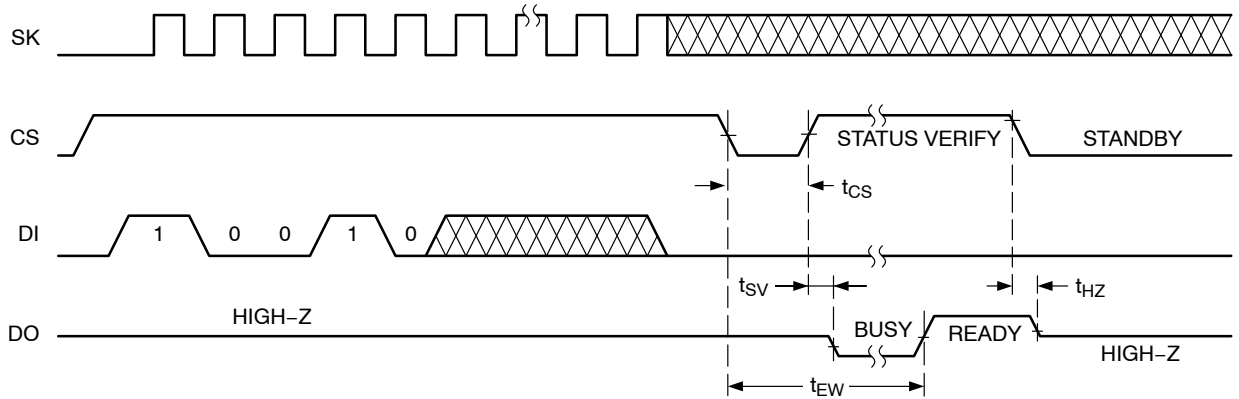


Figure 7. ERAL Instruction Timing

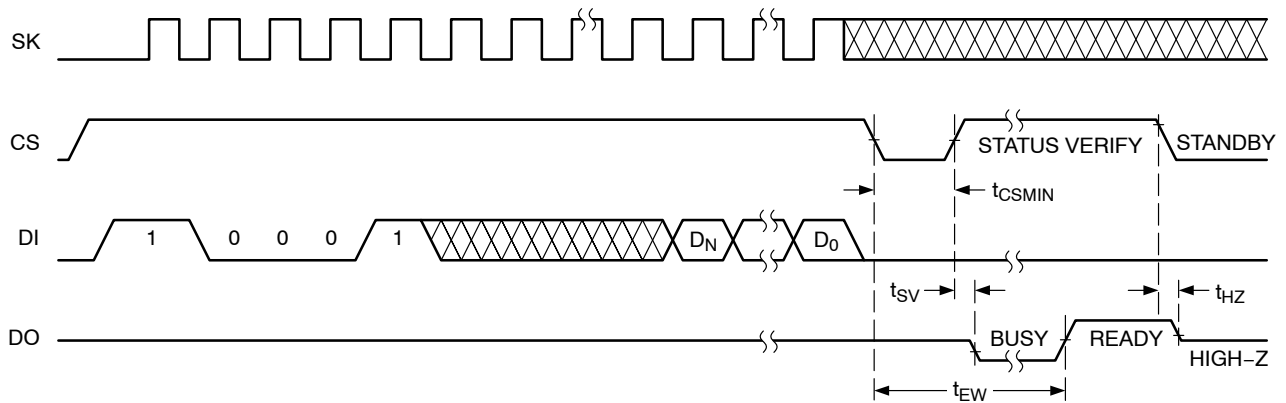
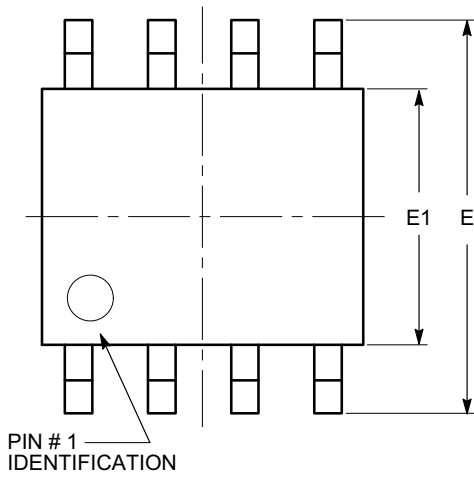


Figure 8. WRAL Instruction Timing

CAV93C66

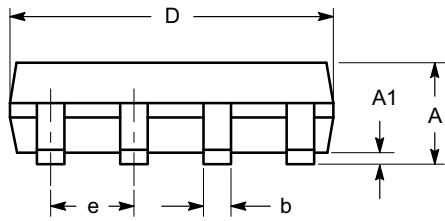
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD-01
ISSUE O

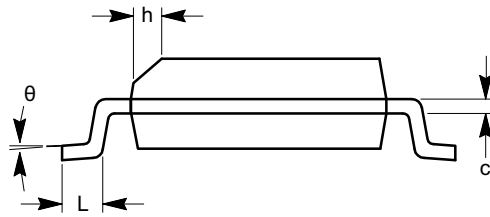


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

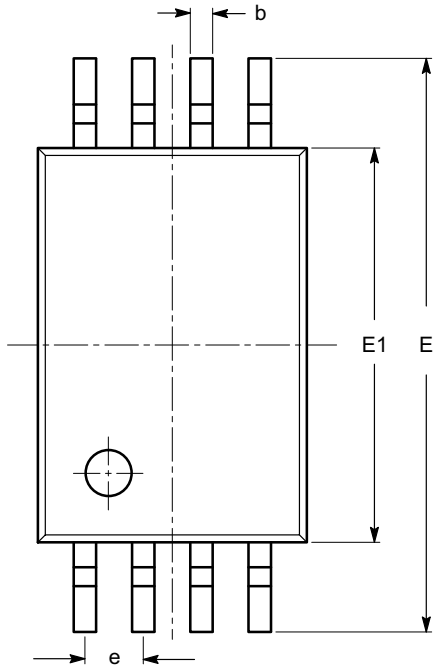
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

CAV93C66

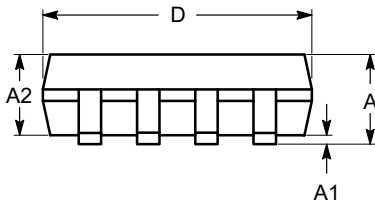
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL-01
ISSUE O

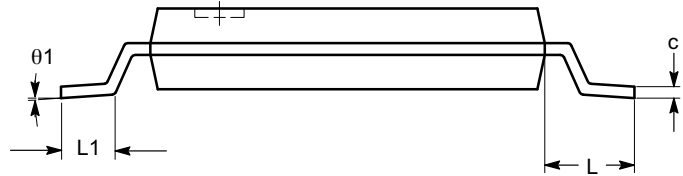


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

Notes:


- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

CAV93C66

Table 9. ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping
CAV93C66VE-GT3	93C66D	SOIC-8, JEDEC	-40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAV93C66YE-GT3	M66D	TSSOP-8	-40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel

8. All packages are RoHS-compliant (Lead-free, Halogen-free).
9. The standard lead finish is NiPdAu.
10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
11. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative